IN THE CLAIMS

1. (Currently Amended) A circuit arrangement for protecting a chip arrangement, comprising:

at least one optosensitive detector unit, comprising at least one bipolar transistor, whose output voltage is a measure of the incidence of light on the detector unit, and

at least one comparator unit preceded by the detector unit for comparing the output voltage of the detector unit with a reference voltage, wherein data or functions of the chip arrangement to be protected can be permanently obstructed, erased, blocked, or interrupted in the case of a failure message occurring during comparison of the output voltage of the detector unit with the reference voltage**;**

wherein the at least one bipolar transistor is disposed in a plane of the data or functions to be protected.

2. (Currently Amended) A circuit arrangement as claimed in claim 1, wherein the detector unit is arranged

underneath at least an oxide layer of the chip arrangement~~, or~~

~~substantially in the plane of the data or functions to be protected~~.

3. (Cancelled)

4. (Currently Amended) A circuit arrangement as claimed in claim 1, wherein the detector unit comprises a plurality of spatially arranged bipolar transistors **disposed in the plane of the data or functions to be protected**.

5. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein an emitter of the bipolar transistor is connected to an input, provided for the output voltage, of the comparator unit.

6. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein an emitter of the bipolar transistor is connected to at least a power supply voltage via at least a power supply resistor.

7. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein a collector of the bipolar transistor is connected to ground potential via at least a reference resistor.

8. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein a junction between a base of the bipolar transistor and a collector of the bipolar transistor is provided for absorbing the light incident on the detector unit.

9. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein the output voltage of the detector unit depends on a wavelength or an intensity of the incident light.

10. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein

at least an evaluation unit is implemented or integrated in the comparator unit, or

the comparator unit precedes at least an evaluation unit.

11. (Previously Presented) A circuit arrangement as claimed in claim 10, wherein the evaluation unit generates the failure message when the output voltage of the detector unit deviates from a nominal range.

12. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein

a working point of the detector unit or

a threshold value of the reference voltage is adjustable.

13. (Previously Presented) A circuit arrangement as claimed in claim 1, further comprising at least a dielectric coating or a further protective coating for protecting the chip arrangement from external influences is arranged within the chip arrangement or laterally to the chip arrangement or on the chip arrangement.

14. (Previously Presented) A circuit arrangement as claimed in claim 13, wherein a material of the protective coating is selected from the group consisting of epoxy resin, silicon nitrite ($SiNO_2$), and silicon dioxide (SiO_2).

15. (Previously Presented) A circuit arrangement as claimed in claim 13, wherein a material of the protective coating is substantially opaque.

16. (Previously Presented) A circuit arrangement as claimed in claim 1, wherein the chip arrangement is arranged on at least a layered carrier substrate of a semiconducting or insulating material.

17. (Currently Amended) A circuit arrangement as claimed in claim 1, ~~wherein the circuit arrangement is implemented or integrated in a card~~ **further comprising a substrate in the form of a card in which the circuit arrangement is disposed**.

18. (Cancelled)

19. (Currently Amended) A chip arrangement, comprising

~~at least one~~ **a plurality of** optosensitive detector unit**s, each optosensitive detector unit comprising at least one bipolar transistor, whose output voltage is a measure of the incidence of light on the detector unit, and at least one comparator unit preceded by the detector unit for comparing the output voltage of the detector unit with a reference voltage, wherein data or functions of the chip arrangement to be protected can be permanently obstructed, erased, blocked, or interrupted in the case of a failure message occurring during comparison of the output voltage of the detector unit with the reference voltage; and wherein the at least one bipolar transistor is disposed in the plane of the data or functions to be protected** ~~as claimed in claim 1~~, and

at least a combination logic unit for combining the **plurality of** detector units **disposed in the chip arrangement**.

20. (Previously Presented) A chip arrangement as claimed in claim 19, wherein the combination logic unit is connected to at least a control logic unit.

21. (Previously Presented) A chip arrangement as claimed in claim 19, wherein the combination logic unit is connected to an electrically erasable storage unit.

22. (Previously Presented) A chip arrangement as claimed in claim 21, wherein the storage unit is constituted by at least an Electrically Erasable Programmable Read-Only Memory (EEPROM) storage unit, and the data or functions of the chip arrangement to be

protected are erasable when a failure message by means of the EEPROM storage unit occurs during comparison of the output voltage of the detector unit with the reference voltage.

23. (Previously Presented) A chip arrangement as claimed in claim 20, wherein

the storage unit is arranged between the combination logic unit and the control logic unit, and

access to the data or functions of the chip arrangement to be protected can be blocked by blocking the storage unit when a failure message occurs during comparison of the output voltage of the detector unit with the reference voltage.

24. (Previously Presented) A chip arrangement as claimed in claim 19, wherein the chip arrangement can be permanently short-circuited via the power supply voltage.

25. (Currently Amended) A method of protecting a chip arrangement, wherein

an output voltage determined by light incident on a detector unit is generated in an optosensitive detector unit comprising a bipolar transistor**, wherein the bipolar transistor is disposed in a plane of the data of functions to be protected**;

the output voltage of the detector unit is compared with a reference voltage in a comparator unit preceded by the detector unit, and

the data or functions of the chip arrangement to be protected are permanently obstructed, erased, blocked, or interrupted when a failure message is generated during comparison of the output voltage of the detector unit with the reference voltage.

26. (Previously Presented) A method as claimed in claim 25, wherein the light incident on the detector unit is substantially absorbed by means of a junction between a base of the bipolar transistor and a collector of the bipolar transistor.

27. (Previously Presented) A method as claimed in claim 25, wherein the failure message is triggered in the comparator unit when the output voltage of the detector unit deviates from a nominal range.

28. (Previously Presented) A method as claimed in claim 25, wherein the triggering of the failure message is adjusted by means of

a working point of the detector unit or

a threshold value of the reference voltage.

29. (Previously Presented) A method as claimed in claim 25, wherein the failure message is generated in at least

an evaluation unit implemented or integrated in the comparator unit, or

an evaluation unit preceded by the comparator unit.

30. (Previously Presented) A method as claimed in claim 25, wherein a control logic unit connected to a combination logic unit provided for combining the detector units is blocked when the failure message is triggered.

31. (Previously Presented) A method as claimed in claim 25, wherein an electrically erasable storage unit arranged between at least a combination logic unit provided for

combining the detector units and a control logic unit is permanently blocked when the failure message is triggered.

32. (Previously Presented) A method as claimed in claim 31, wherein the control logic unit is permanently blocked by means of at least a reset.

33. (Previously Presented) A method as claimed in claim 25, wherein a once-electrically programmable storage unit connected to a combination logic unit provided for combining the detector units is permanently blocked when the failure message is triggered.

34. (Previously Presented) A method as claimed in claim 33, wherein the power supply voltage is short-circuited by means of the storage unit.

35. (Previously Presented) A method as claimed in claim 25, wherein the data or functions to be protected are erased in an Electrically Erasable Programmable Read-Only Memory (EEPROM) storage unit connected to a combination logic unit provided for combining the detector units when the failure message is triggered.